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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,128	JOURDAN ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2002 and 08 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/08/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been examined.

Papers Received

2. Receipt is acknowledged of application, declaration, drawings, information disclosure statement, and change of address papers submitted, where the papers have been placed of record in the file.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "80a" has been used to designate both a fetch block and an entire series of steps in figures 2B and 2C.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "80c" has been used to designate both a fetch block and a fetch block in figure 2D-1.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "80d" has been used to designate both a retire block and a push block in figure 2D-2.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "120" has been used to designate both a decrement block in figure 2C and a push block in figure 2D-1.

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "140a" has been used to designate both a fetch block and an entire series of steps in figure 3B-1.

8. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "140b" has been used to designate both a fetch block and an entire series of steps in figure 3B-2.

9. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "140c" has been used to designate both a fetch block and a push block in figure 3C-1.

10. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "140d" has been used to designate both a retire block and a push block in figure 3C-2.

11. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "140e" has been used to designate both a retire block and a decrement block in figure 3C-2.

12. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "140f" has been used to designate both a decision block and an entire series of steps in figure 3C-4.

13. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required

corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

14. Claim 3 is objected to because of the following informalities: the claim states that "return predicted RETURN addresses" are used "to allow recovery of predicted RETURN addresses in the case of mis-predicted instruction fetching." It is unclear what "return predicted RETURN addresses" are. The examiner is taking the phrase to mean "predicted RETURN addresses" based on the specification. Appropriate correction is required.

15. Claims 4, 6, 8, 18, and 26 are objected to because of the following informalities: a claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Claim Rejections - 35 USC § 112

16. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

17. Claims 3, 10-11, 19, and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

18. Claim 3 recites the limitation "the return address buffer" in lines 18-19 of page 17. There is insufficient antecedent basis for this limitation in the claim. The parent claim

recites three separate return address buffers and it is unclear which is being spoken of. The examiner is taking the claim to mean "the committed address buffer" as set forth in the corresponding claims of the other groups.

19. Claim 10 recites the limitation "the back address" in line 6 of page 20. There is insufficient antecedent basis for this limitation in the claim. A back address has not been defined in the claims to this point nor does the examiner understand what Applicant is trying to claim. The examiner is taking the claim to mean "...and the read pointer is set equal to the next address from the entry being used."

20. Claim 19 recites the limitation "the back address" in line 10 of page 23. There is insufficient antecedent basis for this limitation in the claim. A back address has not been defined in the claims to this point nor does the examiner understand what Applicant is trying to claim. The examiner is taking the claim to mean "...set the read pointer equal to the next address from the entry being read."

21. Claim 27 recites the limitation "the back address" in line 3 of page 26. There is insufficient antecedent basis for this limitation in the claim. A back address has not been defined in the claims to this point nor does the examiner understand what Applicant is trying to claim. The examiner is taking the claim to mean "...setting the read pointer equal to the next address from the entry being read."

Claim Rejections - 35 USC § 102

22. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

23. Claims 1-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Gochman (5,964,868).

24. In regard to claim 1, Gochman discloses an apparatus for storing predicted return addresses of instructions being executed by a pipelined processor, the apparatus comprising:

a. a two part return address buffer, comprising

b. a speculative return address buffer;

c. and a committed return address buffer, both of which having multiple entries that may include predicted return addresses that have been pushed onto the return buffer.

[Gochman has shown in the abstract that a two-part return stack buffer is used. The two-part buffer includes a speculative return stack buffer and an actual return stack buffer. Column 3, lines 50-53 show that the actual return stack buffer is updated with information from fully executed or committed instructions and thus is a committed return buffer. Column 4, lines 38-40 show that the speculative return buffer contains addresses and lines 60-63 show that the actual or committed return buffer contains addresses as well and thus both buffers are address buffers. Further lines 38-40 show that the speculative return address buffer contains predicted return addresses. Since the claim language states that both return address buffers may include predicted return addresses, the actual or committed return address buffer does not need to contains

such predicted addresses and the limitation is met. Figure 1 shows that the buffers have multiple entries.]

25. In regard to claim 2, Gochman discloses the apparatus of claim 1 wherein when a predicted return address stored in the two part return buffer is popped, the predicted return address may come from either the speculative return address buffer or the committed address buffer. [Column 6, lines 48-54 show that a predicted address is fetched or popped from the speculative return address buffer.]

26. In regard to claim 3, Gochman discloses the apparatus of claim 1 wherein the two-part return address buffer stores predicted RETURN addresses to allow recovery of predicted RETURN addresses in the case of mis-predicted instruction fetching. [Column 5, lines 6-18 show that the actual or committed return address buffer copies it's contents into the speculative return address buffer when there is a branch mis-prediction or mis-predicted fetching. Thus the predicted return addresses of the speculative return address buffer are restored. Since, as shown above, all addresses in the speculative return address buffer are for prediction they are predicted values and thus these predicted values are stored in the committed return address buffer.]

27. In regard to claim 4, Gochman discloses the apparatus of claim 2 further comprising:

a. a read pointer pointing to a first entry in the speculative buffer; [Figure 1 shows that the speculative buffer (51) has a TOS (top-of-stack) pointer (53). Column 6, lines 48-54 show that this pointer is used to fetch or read from the stack buffer at the top of the stack (a first entry) and is thus a read pointer.]

b. a write pointer pointing to a second entry in the speculative buffer; [Column 6, lines 33-44 show that the speculative TOS pointer is decremented to point to a second entry and an address is pushed or written to this entry and thus the pointer is also a write pointer.]

c. a processor that executes instructions (figure 4) to:

i. store a first return address in an entry in the speculative buffer, the entry being pointed to by the write pointer; [As shown above]

ii. and read the first return address from the entry in the first set of entries, the entry being pointed to by the read pointer. [As shown above]

28. In regard to claim 5, Gochman discloses the apparatus of claim 4, wherein when a return address is stored in an entry of the speculative buffer the processor executes instructions to:

a. store the read pointer as a back pointer in the same entry, [The examiner is taking the term "back pointer" to simply be a pointer with the name "back" since a "back pointer" is not a standard term of the art. The TOS pointer is inherently stored in some storage entry and in fact in the same entry at all times so the control knows where to get the pointer address from for stack manipulation purposes.]

b. set the read pointer equal to the value of the write pointer, [the value of the read pointer is always set to the value of the write pointer as shown above]

c. and increment the write pointer after the read pointer is set equal to the write pointer. [Column 6, lines 54-56 show that the TOS pointer is incremented.]

29. In regard to claim 6, Gochman discloses the apparatus of claim 2, wherein a number of entries included in the speculative buffer is specified, wherein when the write pointer is incremented above the specified number the write pointer is set to point to the first entry in the speculative buffer. [It is inherent that when the write pointer is incremented above the number of occupied entries in the buffer (a specified number), since the TOS pointer points at the first open entry, that the pointer will be pointing at the first entry in the buffer.]

30. In regard to claim 7, Gochman discloses the apparatus of claim 6, further comprising: a storage device holding an SCOLOR indicator bit that is inverted each time the read pointer is set to point to the first or last entry in the speculative buffer; and a bit storage location associated with each entry in the speculative buffer to hold the current value of SCOLOR each time a return address is written into the speculative buffer. [It is inherent that there exists some indicator bit or bits associated with the buffer (and thus each entry) that tell when the speculative buffer is full (the last entry is pointed to) so that it is known that no more writes to the buffer may be made.]

31. In regard to claim 8, Gochman discloses the apparatus of claim 4, further comprises: retirement logic connected to the apparatus that indicates instructions that have completed execution in the processor, wherein when the retirement logic indicates an instruction has completed execution the return address corresponding to the completed instruction is written from the speculative buffer to the committed buffer. [As shown above, the committed or actual return address buffer indicate instructions that have completed execution in the processor and therefore, this buffer serves as

retirement logic. Column 7, lines 13-18 show that the address of the instruction after a call instruction is copied to the actual return address buffer once the call is executed. This is functionally the same as copying the predicted value from the speculative buffer when the prediction was correct and thus the limitation is disclosed.]

32. In regard to claim 9, Gochman discloses the apparatus of claim 4, further comprising: a storage location holding a pointer indicator bit to indicate the use of the speculative buffer or the committed buffer for reading a return address. [Figure 1 shows that a return address may be selected from either return address buffers. The figure also shows that there are indicator signals or bits (which must be stored somewhere) to indicate the buffer to use.]

33. In regard to claim 10, Gochman discloses the apparatus of claim 9, wherein when the pointer indicator bit indicates the speculative buffer is to be used for reading the return address, the return address is read from the speculative buffer and the read pointer is set equal to the next address from the entry being read. [As shown above and in figure 1, when the speculative buffer is selected, the return address is read from that buffer. As shown previously, the pointer is incremented upon a read from the speculative buffer indicating the address of the next entry.]

34. In regard to claim 11, Gochman discloses the apparatus of claim 10, further comprising:

a. a retirement logic block connected to the apparatus that indicates instructions that have completed execution in the processor, [Actual return address buffer as shown above]

b. wherein when the retirement logic indicates a CALL instruction has completed execution, the return address corresponding to the completed instruction is written from the speculative buffer to the committed buffer. [As shown above]

35. Claim sets 12-19 and 20-27 contain substantially similar limitations and language to claims 1-11 and thus the same arguments presented above apply.

Conclusion

36. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Pat No 5,974,543 to Hilgendorf et al. discloses a processing system that includes a return identification stack and a return cache and thus a two-part return address buffer.

US Pat No 6,374,350 to D'Sa et al. teaches a system and method of maintaining and utilizing multiple return stack buffers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-

4166 after October 12 and (703) 305-7305 before October 12. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162 after October 12 and (703) 305-9712 before October 12. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
September 3, 2004

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